HDI Stackup Guide

Production-oriented stackup patterns, via strategy, and fabrication handoff templates for 4 to 12+ layer HDI boards.

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Prepared by Electuni LLC • Circuit Board Design • circuit-board-design.com

How to use this guide

This is a practical reference for selecting HDI stackups and communicating manufacturable requirements to your PCB fabricator. It favors repeatable, high-yield choices over one-off hero builds. Always confirm capability and targets with the actual fab you will use.

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Key terms

- HDI: High Density Interconnect using fine-line routing plus laser-drilled microvias to increase routing density.
- Microvia: Laser via, typically adjacent-layer only (L1-L2, L2-L3). Yield is best when microvia depth-to-drill is near 1:1.
- Sequential lamination: Building the PCB in stages (1+N+1, 2+N+2, etc.). Each additional lamination cycle increases cost and risk.
- Via-in-pad (VIP): Via placed in a component pad, usually filled and capped to prevent solder wicking (common under BGAs/QFNs).
- Any-layer via: Fabrication process where microvias may be used between any adjacent layers; highest density and highest process control requirements.

When HDI is the right call

- Fine-pitch BGAs (0.8 mm and below), high pin-count SoCs/FPGAs, dense RF modules, and tight fanout channels.
- High-speed buses where you want fewer layer transitions and shorter stubs (or where backdrill is impractical).
- Severe area constraints where through-vias would consume routing real estate or force extra layers.
- Products where repeatability matters: you can lock a proven stackup + via set and reuse it across revisions.

When not to use HDI: If the design can route cleanly with standard through-vias, HDI usually increases cost without improving the electrical outcome. Treat HDI as a tool for density and interconnect, not as a default quality upgrade.

Inputs to lock early

Most HDI failures come from late changes to stackup, footprints, or escape strategy. Lock these before routing:

- Impedance table: targets (e.g., 50 ohm SE, 90/100 ohm diff), tolerance (±10%, ±7%, ±5%), reference plane assignment, and coupon requirement.
- BGA pitch and escape plan: dogbone vs VIP, allowable assembly processes, and whether you will permit stacked microvias.
- Fabricator capability: minimum trace/space, laser via drill + pad diameters, registration class, via fill/cap options, and copper weights available in build-up layers.

- Material choice: FR-4 vs low-loss, Tg requirement, and Dk/Df targets driven by frequency/data rate and insertion loss budget.
- Reliability class: define the expectation (consumer vs industrial vs harsh environment) and whether IPC Class 2/3 style workmanship is required.

Capability and cost drivers

HDI cost is dominated by lamination cycles, via fill requirements, and fine-line yield. The fastest way to stay manufacturable is to constrain the design to a small, repeatable set of rules.

Capability item	Typical range (industry common)	Notes
Laser microvia drill	75-100 um drill, 150-200 um pad	Confirm minimum capture pad and annular ring after registration.
Fine-line trace/space	3/3 mil common; 2/2 mil premium	Yield drops quickly below 3/3; choose only if density forces it.
Stacked microvias	Optional; not always supported	Prefer staggered for yield. Stacked often needs fill + planarization.
Via fill/cap (VIP)	Epoxy fill + cap, or copper fill	Specify method explicitly; affects flatness and assembly yield.
Impedance tolerance	±10% standard; ±7% improved; ±5% premium	Tighter tolerance requires better process control and usually test coupons.

Common HDI stackup patterns

Pattern	Best use case	Manufacturing notes
1+N+1	Entry HDI (6-10 layers)	Microvias on outer build-up layers; core uses through-vias. Best cost/performance starting point.
2+N+2	Higher density / finer BGAs	More routing channels but more lamination cycles. Consider only when 1+N+1 cannot meet escape density.
Any-layer via	Maximum density	Microvias between any adjacent layers. Highest cost; requires strong fab process control and tight DFM alignment.

Rule of thumb: choose the simplest stackup that routes cleanly with margin. Extra build-up layers should be justified by concrete routing density constraints (BGA pitch, escape channels, keepouts), not by preference.