PCB DFM Checklist

A production-focused Design for Manufacturability checklist covering fabrication rules, assembly readiness, panelization, test, and release documentation.

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Prepared by Electuni LLC • Circuit Board Design • circuit-board-design.com

How to use this checklist

Run this checklist twice: (1) during placement/routing to prevent downstream surprises, and (2) before release to ensure your fabrication and assembly package is complete. Targets shown are typical; always confirm with your chosen fabricator/assembler.

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Scope

- Rigid FR-4 PCBs unless otherwise specified.
- Baseline guidance for most products; add project-specific rules for high-speed, high-voltage, or safety-critical designs.
- Where applicable, align workmanship expectations to an IPC class (commonly Class 2 for commercial, Class 3 for high-reliability).

Pre-layout decisions (lock before routing)

☐ Stackup defined (layer count, copper weights, dielectric thicknesses) and agreed with the fab.
☐ Impedance requirements defined (single-ended/differential targets, tolerance, reference planes, coupons).
☐ Fabrication class agreed (standard vs fine-line vs HDI) and minimums documented in design rules.
☐ Assembly process agreed (reflow/wave/selective, lead-free), plus coating/cleanliness/test strategy.
☐ Footprints verified against datasheets and (where available) IPC-7351-style land pattern guidance.

DFM targets snapshot (typical)

Parameter	Standard	Fine-line	HDI
Min trace/space	4/4 mil	3/3 mil	2/2-3/3 mil
Min finished PTH drill	0.20-0.25 mm	0.20 mm	0.15-0.20 mm
PTH aspect ratio	<= 8:1	<= 10:1	<= 10:1 (core)
Microvia depth/drill	N/A	N/A	~1:1 preferred
Min solder mask dam	4 mil	4 mil	3-4 mil
Copper-to-edge	>= 10 mil	>= 10 mil	>= 12 mil

Use these as starting points for design rules and quoting. Your actual fab capability is the source of truth.

Core fabrication checklist

These checks prevent the most common CAM/DFM findings: opens/shorts, drill breakouts, mask failures, warp, and yield loss.

Area	What to verify	Notes
Trace/space	All nets meet minimum width/spacing; critical nets use controlled rules.	Keep margin for yield; avoid pushing minimums unless required.
Copper-to-edge / cutouts	No copper too close to board edge, slots, or routed cutouts.	Common: >= 10 mil copper-to-route; more for edge plating/castellations.
Drills and slots	Finished drills/slots are buildable; NPTH vs PTH clearly defined.	Avoid too many unique drill sizes; separate PTH/NPTH drill files.
Annular ring	Pads maintain annular ring after registration tolerances.	Typical external >= 4 mil; internal >= 3-4 mil (more for high-reliability).
Aspect ratio	PTH aspect ratio within fab capability.	Rule of thumb: board thickness / drill <= 8:1 to 10:1.
Plane antipads	Clearance rules sized correctly for drills in planes/pours.	Include antipad sizing for power/ground planes; check thermal relief rules.
Solder mask	No mask slivers; mask expansion set; via tenting/fill rules defined.	Min mask dam often ~4 mil; define tenting for small vias to reduce wicking.
Silkscreen	Silk does not print on pads; markings are readable and consistent.	Keep silk >= 4-6 mil from exposed copper; use clear polarity markers.
Copper balance	Copper distribution balanced to reduce warp and etch issues.	Use pours/thieving; review each layer for large unbalanced areas.
Return path continuity	Critical signals do not cross plane gaps; stitching vias at transitions.	Avoid splits under fast nets; maintain continuous reference planes.

If you are routing high-speed or RF, add project-specific checks: reference plane continuity, via stub control (backdrill/blind), and connector launch geometry.

Assembly and reliability checklist

Assembly yield is often lost to paste/thermal-pad errors, missing fiducials, and ambiguous polarity/orientation. Check these before release.

Placement, footprints, and paste

☐ Component courtyards/keepouts meet assembly house requirements (especially BGAs, connectors, tall parts).
☐ Fine-pitch footprints reviewed; toe/heel/side fillets match vendor recommendations.
☐ Solder paste apertures reviewed for QFNs, 0.5 mm pitch parts, and large thermal pads (use window-pane where needed).
☐ Thermal pads: via strategy defined (stitch, tent, fill), and paste reduction applied to prevent voiding/float.
☐ Via-in-pad used only when required; fill/cap method specified for any VIP under BGAs/QFNs.

Assembly features and test

☐ Global fiducials present; local fiducials added for fine-pitch BGAs where needed.
☐ Test points provided for power rails, programming/debug, and key nodes; spacing supports pogo pins/fixtures.
☐ Clear polarity/orientation markers for diodes, electrolytics, IC pin-1, connectors, and LEDs.
☐ Mounting holes and mechanical interfaces verified in 3D with enclosure and connector keepouts.
☐ If conformal coating is planned: keepouts and masking requirements documented.

Reliability and safety (as applicable)

- Creepage/clearance meets the applicable standard for your voltage and environment.
- High-current nets sized for temperature rise; copper weight and via stitching support current density.
- If Class 3 workmanship is required, align annular rings, hole sizes, and acceptance criteria accordingly.

Panelization and mechanical

Agree panel strategy early when you have connectors near the edge, heavy parts, or tight pick-and-place constraints.

Panelization

☐ If panelized: rail width, breakaway method (mouse-bites / V-score), and tab locations defined.
☐ Tooling holes and fiducials added on panel rails (or specify assembler-managed panelization).
☐ Keepout zones for depanel tools and conveyors considered (edge clearance for tall parts).
☐ For RF: via fences, controlled edge plating, and edge keepouts specified if required.

Mechanical definition

☐ Board outline, slots, and cutouts are closed and consistent across fab/assembly drawings and CAD exports.
☐ Mounting hole plating (PTH/NPTH), countersinks, and tolerances clearly defined.
☐ Copper keepout from edge/cutouts respected; edge plating/castellations explicitly called out if used.
☐ Solder mask defined at edges (dam/tenting) to avoid exposed copper and assembly shorts.

Release package and final sign-off

A complete release package prevents back-and-forth during CAM and reduces the risk of building the wrong revision.

Fabrication deliverables

- Gerbers/ODB++/IPC-2581 plus drill files (PTH/NPTH separated) and a short readme (units, layer names, revision).
- Stackup table: materials, copper weights, dielectric thickness, impedance callouts, and finished thickness.
- Fabrication drawing: outline/cutouts, tolerances, surface finish (ENIG/HASL/ENEPIG), mask/silk colors, controlled impedance, special processes (via fill/cap, edge plating, backdrill).
- Netlist and DRC report snapshot; document intentional exceptions.

Assembly deliverables

- BOM with manufacturer part numbers (MPNs) and alternates; include DNP/variant notes.
- Assembly drawing with reference designators, polarity/orientation markers, and notes for special parts.
- Centroid/placement file, solder paste layer outputs, and any programming/test instructions.

Final sign-off

☐ Run DRC/ERC; verify all fabrication constraints and plane clearances.
☐ Perform a 3D review: connector alignment, height constraints, keepouts, and mounting.
☐ Do a short peer review focusing on: stackup, vias, mask/paste, polarity markers, and release files.
☐ Request a fab/assembly DFM review when possible; address findings before first build.

References (optional deeper reading)

- IPC-2221 (Printed Board Design)
- IPC-7351 (Surface Mount Land Pattern Standard)
- IPC-A-600 (Acceptability of Printed Boards) and IPC-A-610 (Acceptability of Electronic Assemblies)

Revision history

v1.1 (2026-02-12) - Fixed formatting, added DFM targets snapshot and checkbox-style review flow, expanded assembly and release-package requirements.